REMARKS

Claims 1-2, 4-9, 11-17, 19-24, and 26-28, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-2, 4-9, 11-17, 19-24, and 26-28 again stand rejected under 35 U.S.C. §102(b) as being anticipated by Park, et al. (U.S. Patent No. 6,429,084), hereinafter referred to as Park. Applicants respectfully traverse these rejections based on the following discussion.

Regarding independent claims 1, 9, 16 and 24, Park does not teach or suggest the following features: (1) "forming spacers with a target spacer width adjacent to said gate stack, wherein in order to achieve said target spacer width a combined height of said gate conductor and said at least one sacrificial layer is predetermined" and (2) "wherein said target spacer width is predetermined to ensure that said spacers (or said temporary spacers, see claim 24) sufficiently separate said source and drain regions (or said raised source and drain regions, see claims 9, 16 and 24) from said gate stack so as to avoid lateral encroachment of said impurity into a channel region below said gate stack regardless of a height of said gate conductor." Regarding independent claims 16 and 24 Park also does not teach or suggest the feature "said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities".

The cited prior art and the present invention each provide methods for forming

CMOS transistors with raised source and drain regions; however, the problems addressed are different as are the processes used to solve the problems.

The present invention addresses the problem of encroachment of source/drain dopants into the channel region when gate heights are scaled. That is, with increased scaling of CMOS structures and, specifically, of gate heights, implanting dopants with sufficient energy to dope the source and drain regions and halos using the polygate as a self-aligned mask can cause the dopants to laterally diffuse through the substrate into the channel region as well as penetrate through the poly gate and the gate dielectric into the channel as the gate height is decreased (see paragraphs [0001-0006]). Sidewall spacers are used to avoid lateral encroachment. However, with a shorter gate height, the maximum achievable size of the sidewall spacers is reduced due to the reduced step height for reactive ion etch of a deposited spacer material of a given thickness. Thus, the spacers may not be sufficiently wide enough to avoid lateral encroachment of S/D dopants and also there may be a higher probability of silicide bridging between the gate and the S/D. This problem becomes more severe when using epitaxially grown raised source and drain structures because epitaxial overgrowth occurs on top of the gate with reduced height. The undesirably overgrown epitaxial polysilicon over the gate would also be silicided which would form a conductive path between the gate and the raised source/drain regions, resulting in failure of transistor function. Therefore, as mentioned in paragraphs [0008-10], [0030], [0036], [0039]) of the present application, the method of the invention forms a gate stack with a gate conductor and at least one sacrificial layer. Spacers are then formed with a target spacer width adjacent to that gate stack. The target

spacer width is predetermined to ensure that the spacers sufficiently separate the source and drain regions from the gate stack so as to avoid lateral encroachment of the impurity into the channel region. In order to achieve this target spacer width, regardless of the height of the gate conductor alone, the combined height of the gate conductor and the sacrificial layer(s) is predetermined.

Contrarily, Park addresses the problem of unwanted overgrown epi growth on the gate and STI but not the formation of spacers sufficiently large enough to avoid unwanted lateral diffusion of dopants into channel regions when gate heights are reduced. Specifically, Park discloses a method of forming CMOS transistors with raised source and drain regions (col. 1, lines 5-6). In the Park method a conventional gate stack is formed with several thin sacrificial layers above the 120nm gate conductor (col. 1, lines 58-62). These sacrificial layers protect the surface of the gate conductor during subsequent processing. A protective nitride layer is deposited over the substrate and the gate-sacrificial layers (col. 1, lines 66-67). Temporary spacers are formed on the protective nitride layer against the gate stack and a width of these temporary spacers is "set to define the area for the halo and extensions implants" (col. 2, lines 1-5). A portion of the protective layer 60 above the substrate is etched to define the source and drain regions and then, the temporary spacers are removed (col. 2, lines 25-30). Then, the source and drain regions 34 are implanted, although this step can be omitted if the source and drain regions were previously implanted (col. 2, lines 33-34; see Figure 5). Column 2, lines 34-37 provide that "the layer 60 is thick enough to block the implant in the region that will contain the extension implant." After the source and drain regions 34 are

implanted in the substrate, raised source and drain regions are epitaxially grown (col. 2, lines 43-47; see Figure 7). Unwanted epi growth is prevented by the remaining nitride layer on the gate stack and adjacent to the gate stack in the area of the substrate designated for the S/D extension. Then, after additional processing steps, extension and halo implantation is performed (col. 2, lines 48-64), which also implants the raised epitaxially grown source and drain regions.

Park does not address the issue of lateral encroachment of the impurities (i.e., dopants) from the source and drain regions into the channel because the Park transistor does not have a reduced gate height and, thus, the ability to form spacers with a width sufficient enough to avoid lateral encroachment of the dopants into the channel region was not a problem for Park. Specifically, Park mentions that the widths of the spacers that are formed adjacent to the gate conductor are "set to define the area for the halo and extensions implants" (see col. 2, lines 1-5). Park also indicates that the nitride layer 60 is thick enough to block penetration by the source/drain dopant through the nitride layer down into the area of the substrate designated for the halo and extensions implants (col. 2, lines 34-37) and further discusses the protection provided by sacrificial layers 51, 52 and 54 during subsequent processing. However, the Park gate conductor was disclosed as nominally 120nm thick (see col. 1, lines 57-60) and, thus, those skilled in the art will recognize the gate height was sufficiently tall to achieve spacers with the required target spacer width. Therefore, an alternative technique for achieving the target spacer width was not needed, considered or disclosed. That is, Park does not disclose that sacrificial layers are added to the gate stack in order to achieve a gate stack with a predetermined

combined height that is sufficient for a target spacer width to be achieved because that target spacer width was already achievable. That is, given the gate height of Park, spacers could be made that sufficiently separate the source and drain regions from the gate stack to avoid lateral encroachment of the S/D impurities into the channel region without additional processing.

The Office Action indicates Park avoids lateral encroachment "because the use of the spacer as well dummy spacer is intended to avoid such problem." That may be true; however, the Applicants submit that lateral encroachment is only avoided in Park because the height of the gate conductor was not reduced and, thus, was sufficiently tall to produce spacers with the necessary width. Since no specific accommodations were made for the reduced gate height in Park, if the gate conductor of Park was scaled, the target spacer width necessary to avoid lateral encroachment may or may not be achievable with the Park method. That is, if a "combined height of the gate conductor and the sacrificial layers" is not predetermined so that the target spacer width can be achieved, lateral encroachment of source/drain dopants into the channel region will necessarily occur. Thus, the fact that the Park Figures do not illustrate impurities under the gate conductor is irrelevant because the gate height of Park is not reduced and, so lateral encroachment did not need to be considered. Additionally, support for the fact that lateral diffusion of dopants was not even considered by Park is found in the fact that not only do the drawings fail to show lateral diffusion of impurities into the channel region but also fail to show any lateral diffusion of impurities at all. Those skilled in the art would recognize that such lateral diffusion would necessarily occur to some extent, especially following

the epi growth process. Thus, the lack of lateral dopant diffusion in the Park Figures only supports the fact that lateral diffusion was not considered by Park. It does not support the a finding that Park disclosed that the combined height of the gate stack was predetermined so that spacers with a predetermined target spacer width could be achieved in order to avoid lateral encroachment of the source and drain impurities into the channel region.

Furthermore, regarding independent claims 9, 16 and 24, Park does not teach or suggest "after said epitaxially growing of said raised source and drain regions, implanting an impurity into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurity after said epitaxially growing of said raised source and drain regions avoids subjecting said impurity to the thermal budget of said epitaxially growing process" (see paragraphs [0042] and [0047]). Specifically, Park discloses implanting the source and drain regions in the substrate *before growing the epi* (col. 2, lines 33-48, see Figure 5). The impurities implanted into these source and drain regions in the substrate would necessarily be subjected to the epi process (col. 2, lines 44-48, see Figure 7) with a conventional temperature range from about 750°C-850°C) and, thus, subjected to the deleterious effects of transient enhanced diffusion of impurities, such as boron.

The Office Action cites Figures 9 and 10 as disclosing that the implant to form the S/D extension 35 is conducted after the epitaxial layer is formed. However, the S/D extension 35 is not the same as the source/drain regions 34. Specifically, col. 2, lines 34-40 disclose the implant of source/drain regions 34 in the substrate adjacent to that region

of the substrate that is blocked by nitride 60 and defines the area of the substrate that will contain the extension. After the source/drain regions 34 are implanted into the substrate, the epi process is performed (see col. 2, lines 40-48) and the dopants in the source/drain regions are necessarily subjected to the thermal epi process resulting in diffusion of the s/d dopants. Col. 2, lines 56-58 and associated Figures 9-10 simply disclose that after the epi is grown, a thermal oxide layer is grown on the epi (Figure 9) and a second implant process is used to implant the halos and extensions (Figure 10) to avoid subjecting the halos/extensions to the thermal epi process. Again, the source/drain regions 34 that are *below* the raised source/drain regions 36 of Figures 9-10 were doped prior to the epi process (see Figure 5).

Lastly, regarding independent claim 16 and 24, Park does not teach or suggest "wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities." The Office Action cites Figures 9 and 10 as teaching this feature. However, as mentioned above, Park teaches doping the source and drain regions 34 in the substrate prior to growing the epi on those source and drain regions (see Figures 5-7 and associated text in the Specification). Thus, Park necessarily teaches that the process of epitaxially growing the raised source and drain regions 36 is performed in the presence of doping impurities.

Therefore, the Applicants respectfully submit that independent claims 1, 9, 16, and 24 are patentable over the prior art of record. Further, dependent claims 4-8, 11-15, 17, 19-23 and 26-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the

invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-2, 4-9, 11-17, 19-24, and 26-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

Dated: 4/18/06

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